CLAIMS

What is Claimed is:

1. A silicon carbide semiconductor device comprising:

a semiconductor layer made of silicon carbide;

an electrode provided on the semiconductor layer;

an interlayer dielectric film provided on the electrode; and

an interconnect that passes through the interlayer dielectric film and reaches the electrode,

wherein the electrode comprises: a first electrode portion in contact with the semiconductor layer; and a second electrode portion interposed between the first electrode portion and the interlayer dielectric film.

2. The silicon carbide semiconductor device of Claim 1,

wherein the second electrode portion covers the top face and side faces of the first electrode portion.

3. The silicon carbide semiconductor device of Claim 1,

wherein the first electrode portion is in ohmic contact with the semiconductor layer.

4. The silicon carbide semiconductor device of Claim 1,

wherein the first electrode portion comprises Ni.

5. The silicon carbide semiconductor device of Claim 1,

wherein the second electrode portion comprises at least one of Al, Ti and Cr.

6. The silicon carbide semiconductor device of any one of Claims 1 to 5,

wherein the interlayer dielectric film is made of silicon oxide.

7. The silicon carbide semiconductor device of Claim 1,

wherein a gate electrode is provided over the semiconductor layer.

8. The silicon carbide semiconductor device of Claim 7,

wherein the second electrode portion is made of the same material as the gate electrode.

9. The silicon carbide semiconductor device of Claim 7,

wherein the semiconductor layer is a high resistance layer comprising a dopant of a first conductivity type,

wherein the semiconductor device further comprises:

a semiconductor substrate that is provided on the back side of the semiconductor layer and has a first conductivity type dopant concentration higher than that of the semiconductor layer;

a plurality of well regions each provided in an upper portion of the high resistance layer and comprising a dopant of a second conductivity type;

a contact region of the second conductivity type provided in an upper portion of each well region;

a source region of the first conductivity type provided in an upper portion of each of the plurality of well regions, the upper portion being located to laterally surround the

contact region;

a gate insulating film provided on a portion of the high resistance layer located between the plurality of well regions; and

a drain electrode provided on the back side of the semiconductor substrate,

wherein the electrode is a source electrode that is provided on the contact region and on a part of the source region adjacent thereto, and

wherein the gate electrode is provided on the gate insulating film.

10. The silicon carbide semiconductor device of Claim 9,

wherein the high resistance layer is further provided, at its upper portion, with an accumulation channel layer, and

wherein the gate insulating film is provided on the accumulation channel layer.

11. The silicon carbide semiconductor device of Claim 7,

wherein the semiconductor layer is a base layer comprising a dopant of a second conductivity type,

wherein the semiconductor device further comprises:

a drift layer that is provided on the back side of the semiconductor layer and comprises a dopant of a first conductivity type;

a semiconductor substrate provided on the back side of the drift layer;

a trench that passes through the base layer and reaches the drift layer;

a gate insulating film provided on the side faces of the trench;

a contact region of the second conductivity type provided in an upper portion of the base layer;

a source region provided in an upper portion of the base layer located to laterally

surround the contact region; and

a drain electrode provided on the back side of the semiconductor substrate,

wherein the electrode is a source electrode that is provided on the contact region and on a part of the source region adjacent thereto, and

wherein the gate electrode is provided on the gate insulating film.

12. The silicon carbide semiconductor device of Claim 7,

wherein the semiconductor layer is a base layer comprising a dopant of a second conductivity type,

wherein the semiconductor device further comprises:

a semiconductor substrate provided on the back side of the base layer;

source and drain regions of a first conductivity type provided in upper portions of the base layer so as to be separated from each other; and

a gate insulating film provided on a portion of the base layer located between the source region and the drain region,

wherein the electrode is a source electrode provided on the source region or a drain electrode provided on the drain region, and

wherein the gate electrode is provided on the gate insulating film.

13. The silicon carbide semiconductor device of Claim 7,

wherein the semiconductor layer is a drift layer comprising a dopant of a first conductivity type,

wherein the semiconductor device further comprises:

a semiconductor substrate provided on the back side of the drift layer; and

source and drain regions of the first conductivity type provided in upper portions

of the drift layer so as to be separated from each other,

wherein the electrode is a source electrode provided on the source region or a drain electrode provided on the drain region, and

wherein the gate electrode is provided on a portion of the drift layer located between the source region and the drain region.

14. The silicon carbide semiconductor device of Claim 7,

wherein the semiconductor layer is a drift layer that comprises a dopant of a first conductivity type and has a mesa,

wherein the semiconductor device further comprises:

a semiconductor substrate provided on the back side of the drift layer; and

a source region of the first conductivity type provided in an upper portion of the mesa of the drift layer,

wherein the electrode is a source electrode that is provided on the top face of the mesa of the drift layer so as to be in contact with the source region, and

wherein the gate electrode is provided on each side face of the mesa of the drift layer and on a part of the drift layer located on each side of the mesa.

15. The silicon carbide semiconductor device of Claim 7,

wherein the semiconductor layer is a drift layer comprising a dopant of a first conductivity type,

wherein the semiconductor device further comprises:

a semiconductor substrate provided on the back side of the drift layer;

a source region of the first conductivity type provided in an upper portion of the drift layer; and

gate regions of a second conductivity type provided in upper portions of the drift layer located on both sides of the source region so that the gate regions are separated from the source region,

wherein the electrode is a source electrode provided on the source region, and

wherein the gate electrode is provided on each of the gate regions.

16. A method for fabricating a silicon carbide semiconductor device comprising an element having: a semiconductor layer made of silicon carbide; and an electrode provided on the semiconductor layer, the method comprising the steps of:

a) forming, on the semiconductor layer, a first electrode portion that constitutes a part of the electrode;

b) forming a second electrode portion that covers at least a part of the first electrode portion and constitutes a part of the electrode, after the step a) has been performed;

c) forming, on the semiconductor layer, an interlayer dielectric film that covers the electrode, after the step b) has been performed;

d) forming a hole that passes through the interlayer dielectric film and reaches the electrode, after the step c) has been performed; and

e) forming an interconnect by filling the hole with a conductor, after the step d) has been performed.

17. The fabricating method of Claim 16,

wherein in the step b), a conductor film that covers at least a part of the first electrode portion and extends above the semiconductor layer is formed, and then the conductor film is patterned, thus forming the second electrode portion and a gate electrode.

18. The fabricating method of Claim 16,

wherein in the step b), the second electrode portion is formed so as to completely cover the top face and side faces of the first electrode portion.

19. The fabricating method of Claim 16,

wherein the first electrode portion comprises Ni.

20. The fabricating method of Claim 16,

wherein the second electrode portion comprises at least one of Al, Ti and Cr.

21. The fabricating method of any one of Claims 16 to 20,

wherein the interlayer dielectric film is made of silicon oxide.

22. The fabricating method of Claim 16,

wherein the element is a double implantation MOSFET, a trench MOSFET, a lateral MOSFET, a MESFET, a static induction transistor, or a JFET.